integral™
STORAGE
TECHNICAL DATASHEET

Integral Mini PCIe 70mm

Specification

Version 1.0

Features:

- Standard ATA/IDE Bus Interface
  - 512 Bytes / Sector
  - ATA comm
  - and set compatible
- Capacities
  - **Integral Z Series (MLC)** 16GB, 32GB, 64GB
  - **Integral E Series (SLC)** Please call for availability
- Data Transfer mode
  - Support Data Transfer up to PIO mode 6
  - Support Data Transfer up to Multiword DMA mode 2
  - Support Data Transfer up to Ultra DMA mode 5
- Performance

  Integral Z Series (MLC Flash):

- Sustain Read Speed up to 35MB/s
- Sustain Write Speed up to 15MB/s

  Integral E Series (SLC Flash): Please call for availability

- Sustain Read Speed up to 45MB/s
- Sustain Write Speed up to 35MB/s

- Temperature Ranges
  - 0^0C to 70^0C for operating
  - -25^0C to 85^0C for storage
- Operating Voltage
  - 3.3V
- Intelligent ATA/IDE Module
  - Built-in Embedded Flash File System
  - Implements dynamic wear-leveling algorithms and static wear-leveling algorithms to increase endurance of flash media
  - Built-in ECC corrects up to 12 random bits error per 512 bytes
- RoHS Compliance

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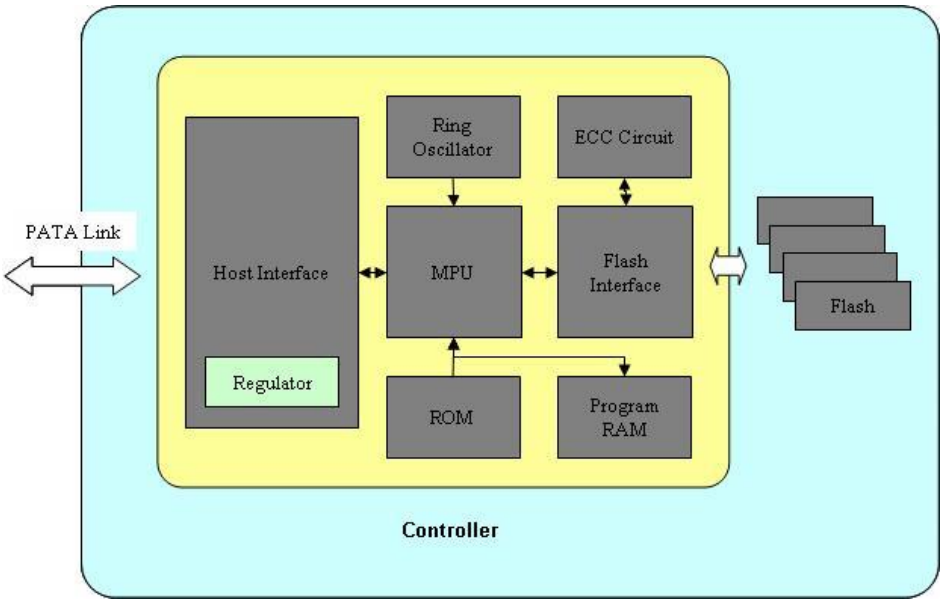
1.0 Block Diagram

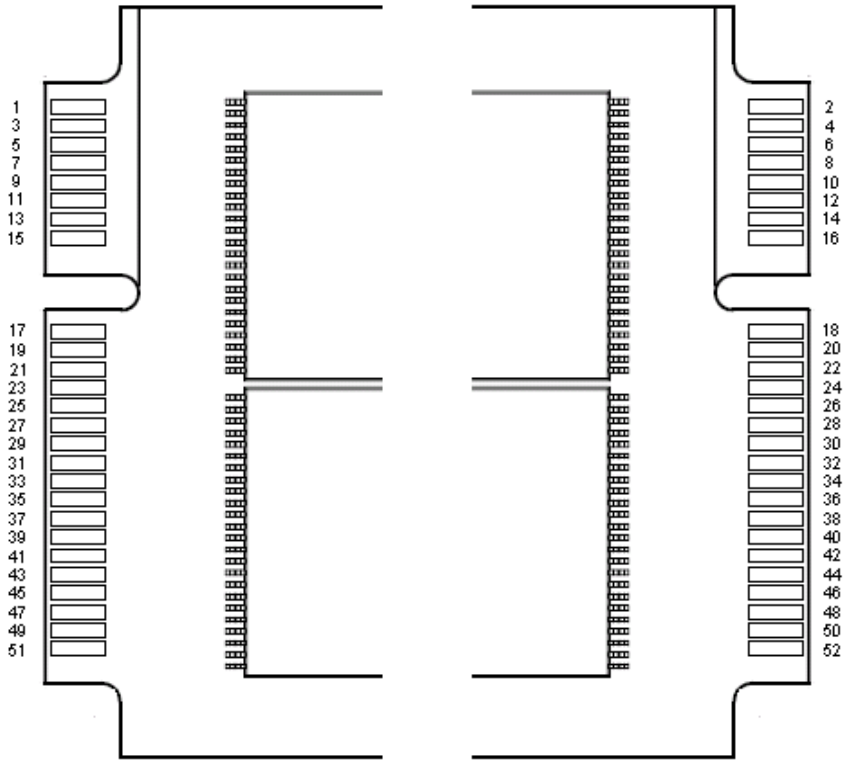


1.1 Capacity Specification

Density	Total Bytes	Cylinders	Heads	Sectors
16GB	16,441,270,272	16383	16	63
32GB	32,279,224,320	16383	16	63
64GB	64,558,448,640	16383	16	63

2.0 Specification

2.1 Pin Assignments



Pin Number	Signal	Pin Number	Signal
1	HD0	2	HD15
3	HD1	4	GND
5	HD2	6	HD14
7	HD3	8	HD13
9	GND	10	HD12
11	HD4	12	HD11
13	HD5	14	HD10
15	GND	16	HD9
17	HD6	18	GND
19	HD7	20	HD8
21	GND	22	nHRESET
23	NC	24	nHIOW
25	NC	26	CSEL
27	GND	28	nHIOR
29	GND	30	nDMACK
31	NC	32	DMARQ

33	NC	34	GND
35	GND	36	NC
37	HA0	38	NC
39	HA1	40	GND
41	HA2	42	IORDY
43	nIOIS16	44	INTRQ
45	nPDIAG	46	nHCS0
47	3V3	48	nHCS1
49	3V3	50	GND
51	3V3	52	nDASP

2.2 Pin Description

Pin No.	Signal	I/O*	Description
22	**-RESET**	**I**	**Hardware reset signal from the host**
1, 3, 5, 7, 11, 13, 17, 19, 20, 16, 14, 12, 10, 8, 6, 2	**HD0~HD15(Device Data)**	**I/O**	**16-bit bi-direction Data Bus. DD(7:0) are used for 8-bit register transfers.**
32	**DMARQ(DMA Request)**	**O**	**For DMA data transfers. Device will assert DMARQ when the device is ready to transfer data to or from the host.**
24	**-DIOW(I/O Write)**	**I**	**This is the strobe signal used by the host to write to the device register or Data port**
	STOP(Stop UDMA Burst)		**The host assert this signal during an UDMA burst to stop the DMA burst**
42	**IORDY(I/O channel ready)**	**O**	**This signal is used to temporarily stop the host register access (read or write) when the device is not ready to respond to a data transfer request.**
	DDMARDY(UDMA ready)		**The device will assert this signal to indicate that the device is ready to receive UDMA data-out burst.**
	DSTROBE(UDMA data strobe)		**When UDMA mode DMA Read is active, this signal is the data-in strobe generated by the device.**
26	**CSEL(Cable select)**	**I**	**This pin is used to configure this device**

			as Device 0 or Device 1.
30	**-DMACK(DMA acknowledge)**	**I**	**This signal is used by the host in respond to DMARQ to initiate DMA transfer.**
44	**INTRQ(Interrupt)**	**O**	**When this device is selected, this signal is the active high Interrupt Request to the host**
43	**IOIS16**	**O**	**During PIO transfer mode0,1or 2, this pin indicates to the host the 16-bit data port has been addressed and the device is prepared to send or receive a 16-bit data word.** **When transferring in DMA mode, the host must use a 16-bit DMA channel and this signal will not be asserted.**
37, 39, 41	**HA0~HA2(Device Address)**	**I**	**This is 3-bit binary coded Address Bus.**
45	**-PDIAG(Passed diagnostics)**	**I/O**	**This signal will be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics,**
	-CBLID(Cable assembly type identify)		
46,48	**-CS0, -CS1(Chip select)**	**I**	**These signals are used to select the Command Block and Control Block registers. When –DMACK is asserted, -Cs0 and –Cs1 shall be negated and transfers shall be 16-bit wide.**
52	**-DASP(Device active, Device 1 present)**	**I/O**	**During the reset protocol, -DASP shall be asserted by Device 1 to indicate that the device is present.**
47, 49, 51	**VCC**	**P**	**Power supply**
9, 15, 21, 27, 29, 35, 4, 18, 26, 34, 40, 50	**GND**	**--**	**Ground.**

***Note:**

"I"	An input from the host system to the device.
"O"	An output from the device to the host system.
"I/O"	An input/output(bi-direction) common.
"P"	Power supply.

3.0 Electrical Characteristics

3.1 Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V
2	VIN	Input Voltage	Vss-0.3	V_{DD}+0.3	V
3	Ta	Operating Temperature	0	+70	^{0}C
4	Tst	Storage Temperature	-25	+85	^{0}C

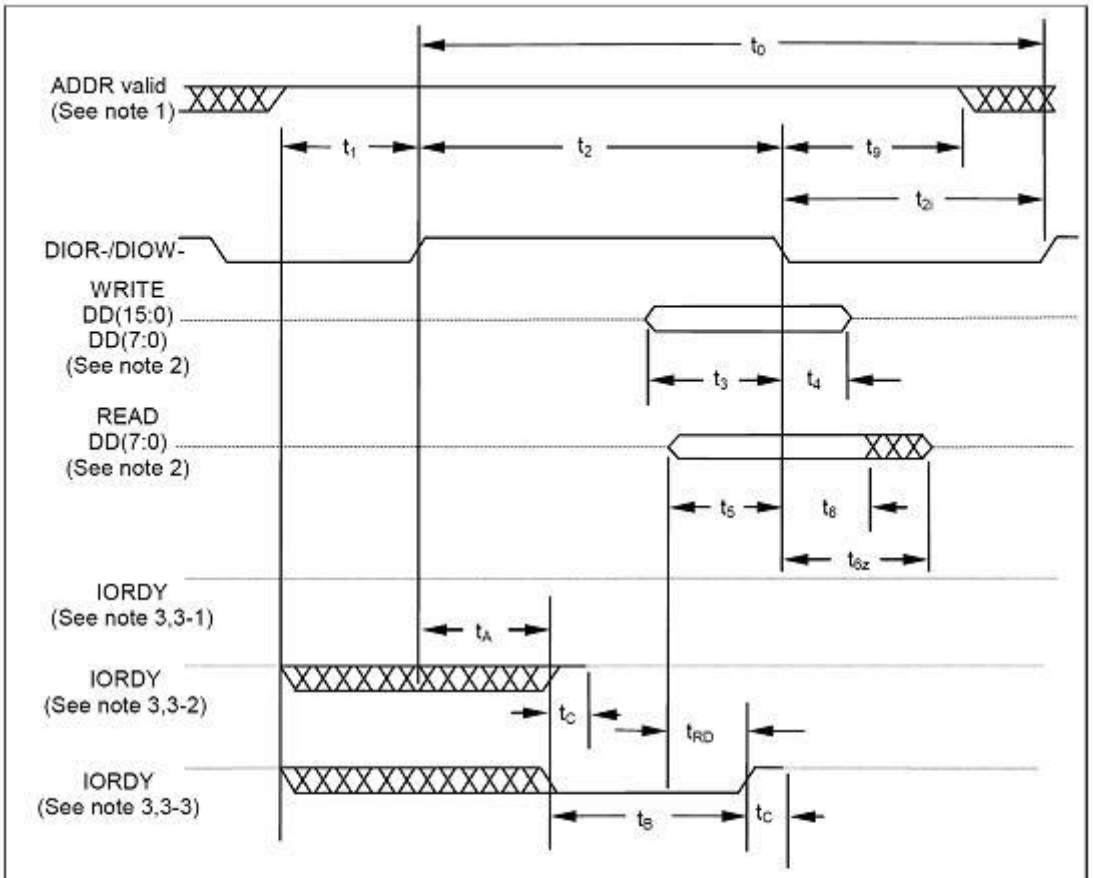
Parameter	Symbol	MIN	TYP	MAX	Unit
V_{DD} Voltage	V_{DD}	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

3.2 DC Characteristics of 5.0V I/O Cells(Host Interface)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Vil	Input Low Voltage	TTL(5V)	--	--	0.85	V
Vih	Input High Voltage		1.25	--	--	V
Vil	Input Low Voltage	TTL(3.3V)	--	--	1.05	V
Vih	Input High Voltage		1.75	--	--	V
Vol	Output Low Voltage	|Iol| = 4~32 mA	--	--	0.4	V
Voh	Output High Voltage	|Ioh|= 4~32 mA	2.4	--	--	V
Iin	Input Leakage Current	No pull-up or pull down	-10	±1	10	μA
Ioz	Tri-state Output Leakage Current		-10	±1	10	μA

3.3 AC Characteristics

3.3.1 PIO Data Transfer



NOTES –

1 Device address consists of signals CS0-, CS1-, and DA(2:0)

2 Data consists of DD(7:0).

3 The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

- 3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
- 3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
- 3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.

4 DMACK- shall remain negated during a register transfer.

PIO timing parameters		Mode 0 ns	Mode 1 ns	Mode2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time (min)	600	383	240	180	120	1,4
t_1	Address valid to DIOR-/DIOW- setup (min)	70	50	30	30	25	
t_2	DIOR-/DIOW- (min)	165	125	100	80	70	1
t_{2i}	DIOR-/DIOW- recovery time (min)	--	--	--	70	25	1
t_3	DIOW- data setup (min)	60	45	30	30	20	
t_4	DIOW- data hold (min)	30	20	15	10	10	
t_5	DIOR- data setup (min)	50	35	20	20	20	
t_6	DIOR- data hold (min)	5	5	5	5	5	
t_{6z}	DIOR- data tristate (max)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold (min)	20	15	10	10	10	10
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A) (min)	0	0	0	0	0	
t_A	IORDY Setup time	35	35	35	35	35	3
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release (max)	5	5	5	5	5	

Notes-

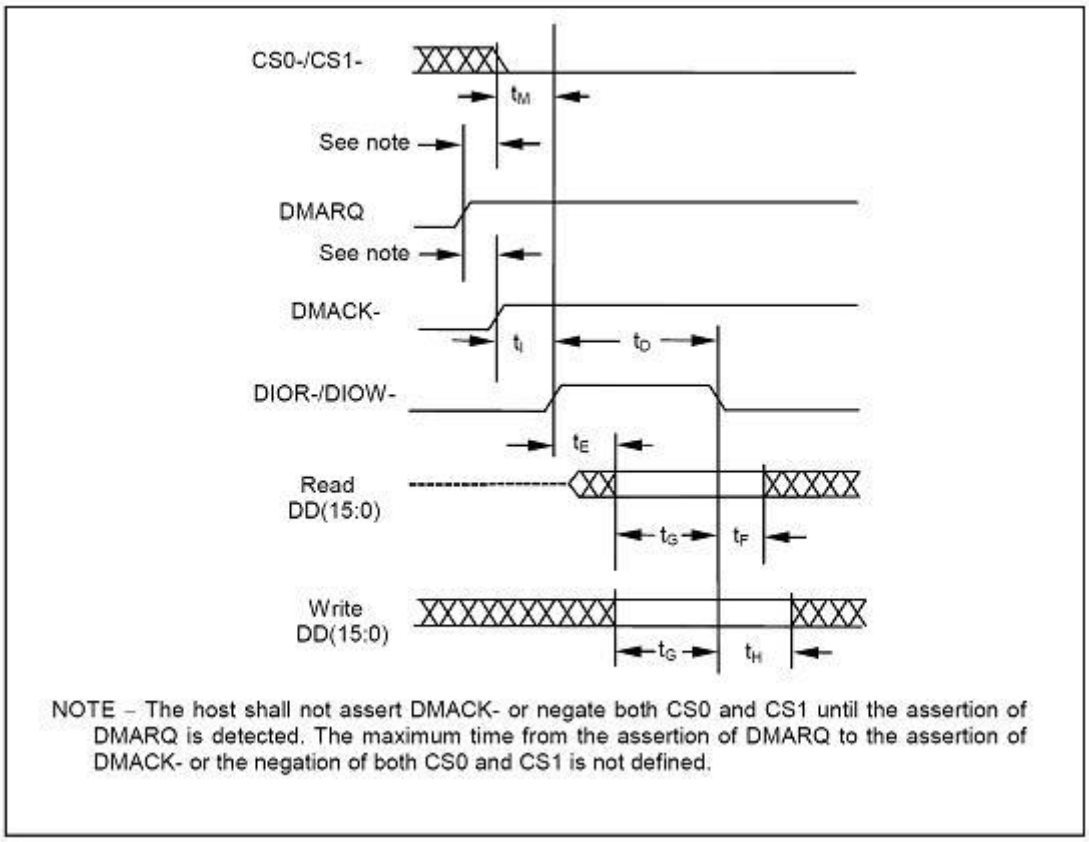
1. **t_0 is minimum total cycle, t_2 is minimum DIOR-/DIOW- assertion time, and t_{2i} is the minimum DIOR-/DIOW- negation time. A host implementation shall lengthen t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any length host implementation.**
2. **This parameter specifies the time from the negation edge of DIOR- to the time that the data is released by the device.**
3. **The delay from the activation of FIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is complete. If the device is not driving IORDY negated at the t_A after the activation of DIOR-**

or DIOW-, that t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY

negated at the time t_A after the activation of DIOR- or DIOW-, then tRD shall be met and t_5 is not applicable.

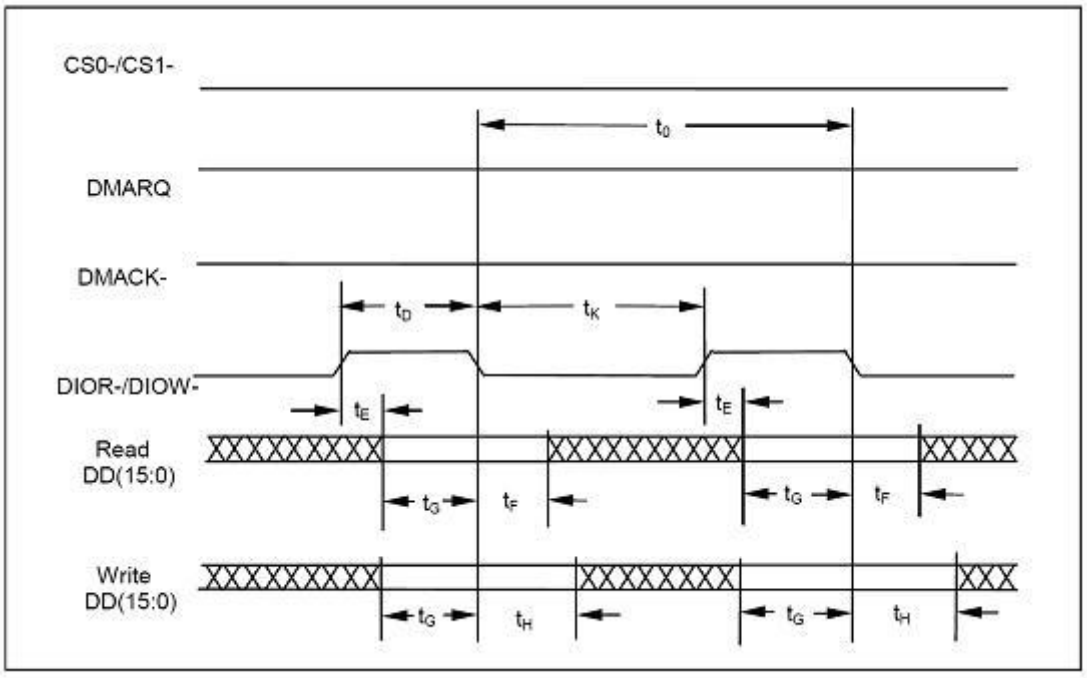
4. Mode may be selected at the highest mode for the device if CS(1:0) and DA(2:0) do not change between read or write cycle or selects at the highest mode supported by the slowest device if CS(1:0) and DA(2:0) do change between read or write cycles.

3.3.2 Multiword DMA Data Transfer

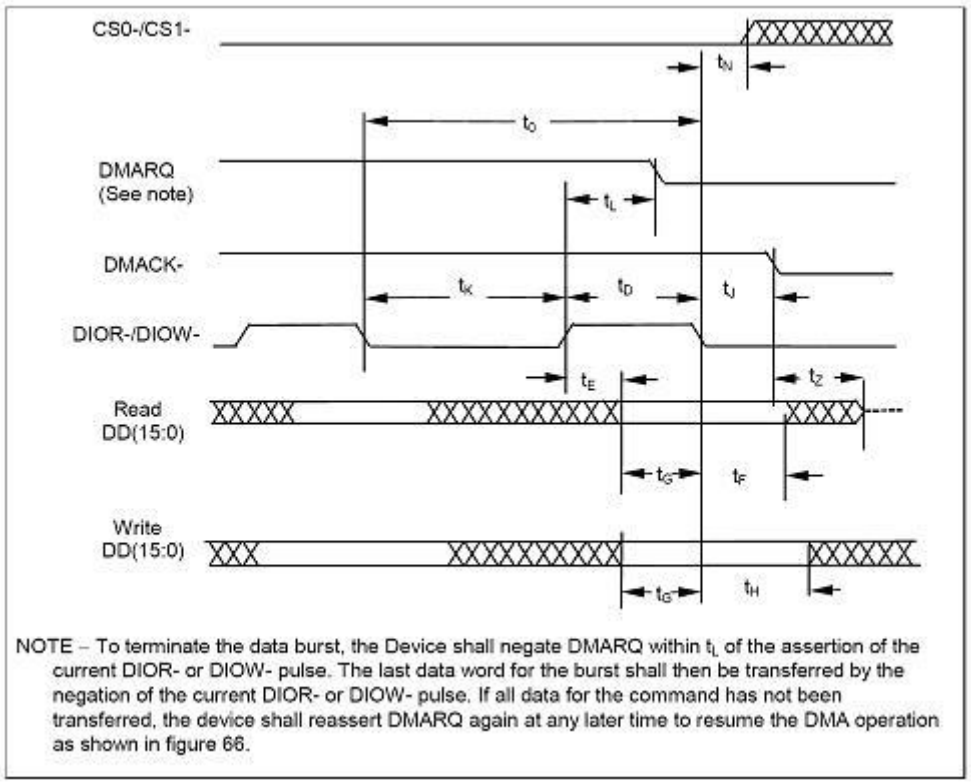


NOTE – The host shall not assert DMACK- or negate both CS0 and CS1 until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK- or the negation of both CS0 and CS1 is not defined.

(Initialing a Multiword DMA data burst)

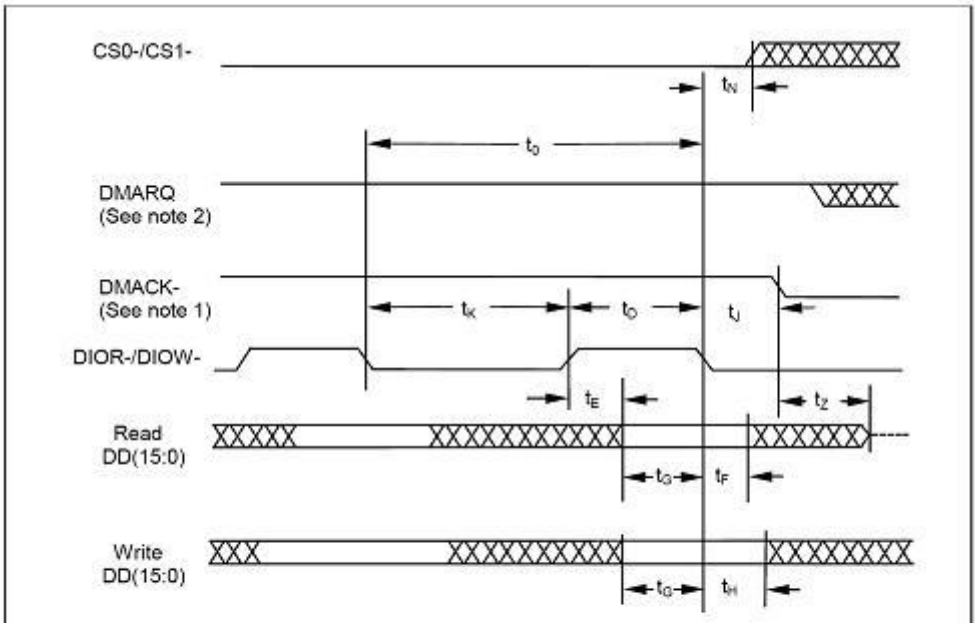


(Sustaining a Multiword DMA data burst)



NOTE – To terminate the data burst, the Device shall negate DMARQ within t_L of the assertion of the current DIOR- or DIOW- pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR- or DIOW- pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation as shown in figure 66.

(Device terminating a Multiword DMA data burst)



NOTE –

1 To terminate the transmission of a data burst, the host shall negate DMACK- within t_J after a DIOR- or DIOW- pulse. No further DIOR- or DIOW- pulses shall be asserted for this burst.

2 If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK- or may negate DMARQ at any time after detecting that DMACK- has been negated.

(Host terminating a Multiword DMA data burst)

Multiword DMA timing parameters			Mode 0 ns	Mode 1 ns	Mode2 ns	Note
t_0	Cycle time	(min)	480	150	120	See note
t_D	DIOR-/DIOW- asserted pulse width	(min)	215	80	70	See note
t_E	DIOR- data access	(max)	150	60	50	
t_F	DIOR- data hold	(min)	5	5	5	
t_G	DIOR-/DIOW- data setup	(min)	100	30	20	
t_H	DIOW- data hold	(min)	20	15	10	
t_I	DMACK to DIOR-/DIOW- setup	(min)	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold	(min)	20	5	5	
t_{KR}	DIOR- negated pulse width	(min)	50	50	25	See note
t_{KW}	DIOW- negated pulse width	(min)	215	50	25	See note
t_{LR}	DIOR- to DMACK delay	(max)	120	40	35	
t_{LW}	DIOW- to DMACK delay	(max)	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW-	(min)	50	30	25	
t_N	CS(1:0) hold	(min)	15	10	10	
t_Z	DMACK- to read data released	(max)	20	25	25	

Notes- t_0 is the minimum total cycle. t_D is the minimum DIOR-/DIOW- assertion time, and t_K(t_{KR} or t_{KW}, as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_K to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data.

3.3.3 Ultra DMA Data Transfer

Ultra DMA data burst timing requirements

Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Mode 5 (in ns)		Mode 6 (in ns)		Measurement location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		30		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		Note 3
t_{2CYC}	230		153		115		86		57		38		29		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		Sender
t_{FS}		230		200		170		130		120		90		80	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60	Note 4
t_{MLI}	20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		50		Sender

NOTES –

1 All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2 All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and DMARDY- transitions are measured at the sender connector.

3 The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

4 The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5 The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.

Ultra DMA data burst timing descriptions

Name	Comment
$t_{2CYCTYP}$	Typical sustained average two cycle time
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until STROBE edge) (See note 2,5)
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid) (See note 2,5)
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge) (See note 3)
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid) (See note 3)
t_{CS}	CRC word setup time at device (See note 2)
t_{CH}	CRC word hold time device (See note 2)
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK- negation) (See note 3)
t_{CVH}	CRC word valid hold time at sender (from DMACK- negation until CRC may become invalid) (See note 3)
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time (See note 1)
t_{MLI}	Interlock time with minimum (See note 1)
t_{UI}	Unlimited interlock time (See note 1)
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	drivers to assert or negate (from released)
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY (See note 4)
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

NOTES –

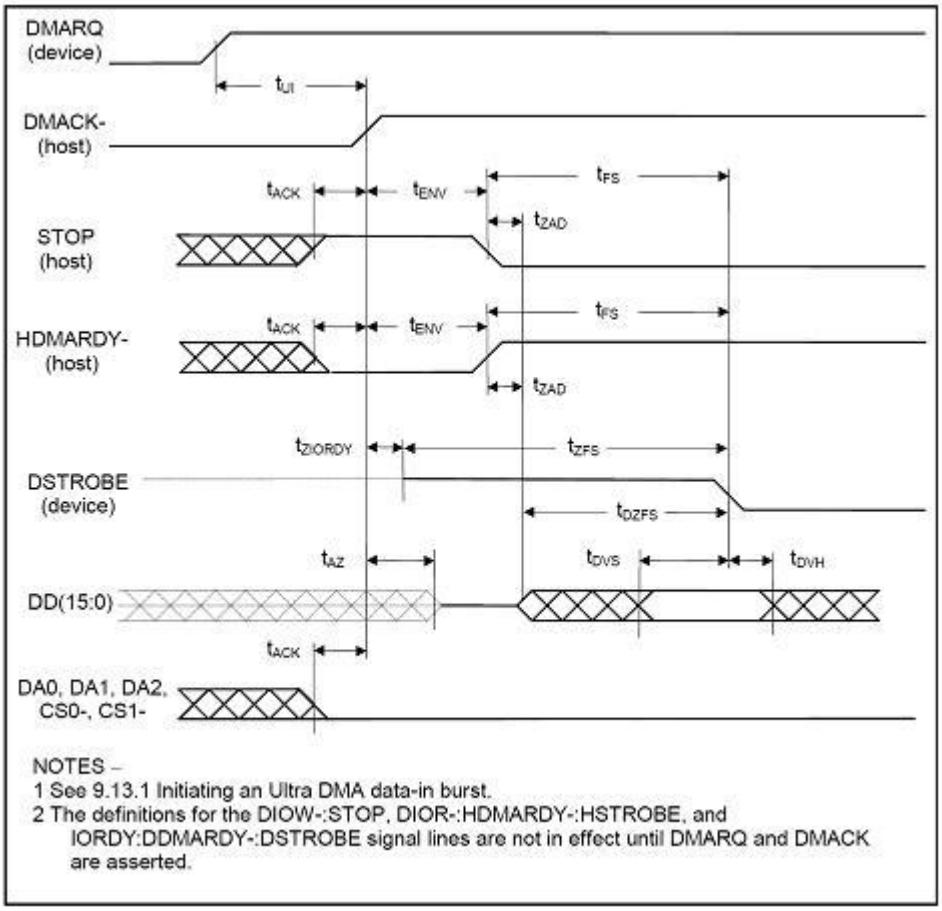
1 The parameters t_{UI}, t_{MLI} (in Figure 74 and Figure 75), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

2 80-conductor cabling (See 7.3) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

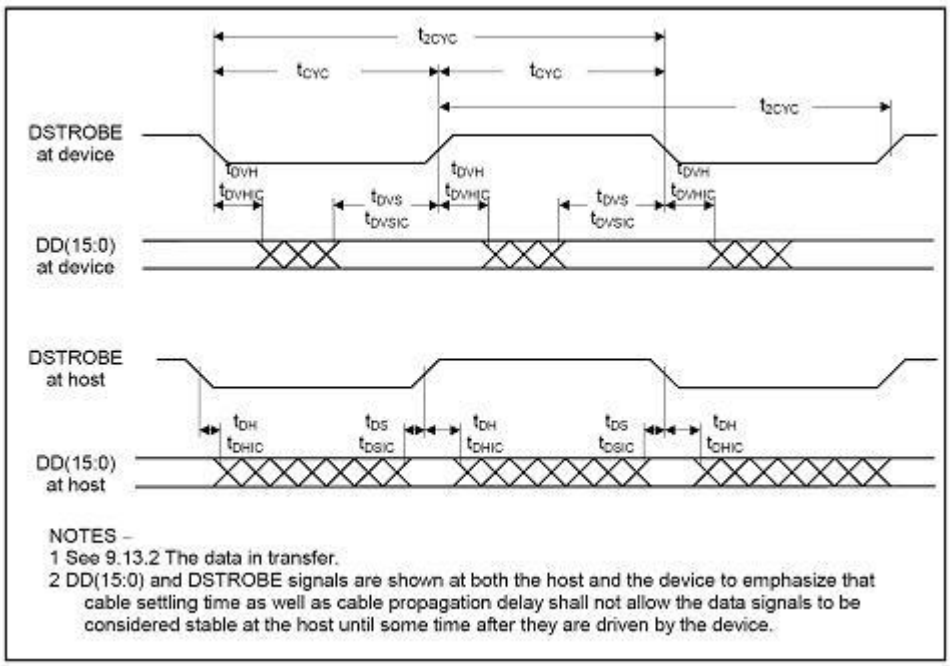
3 Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4 For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

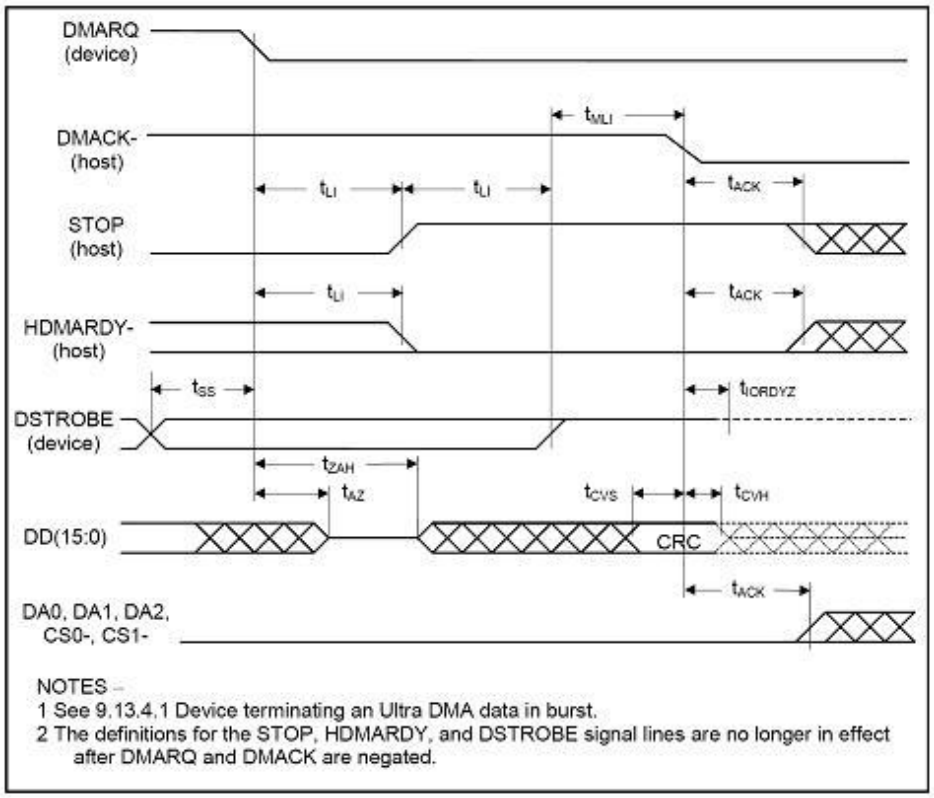
5 The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.



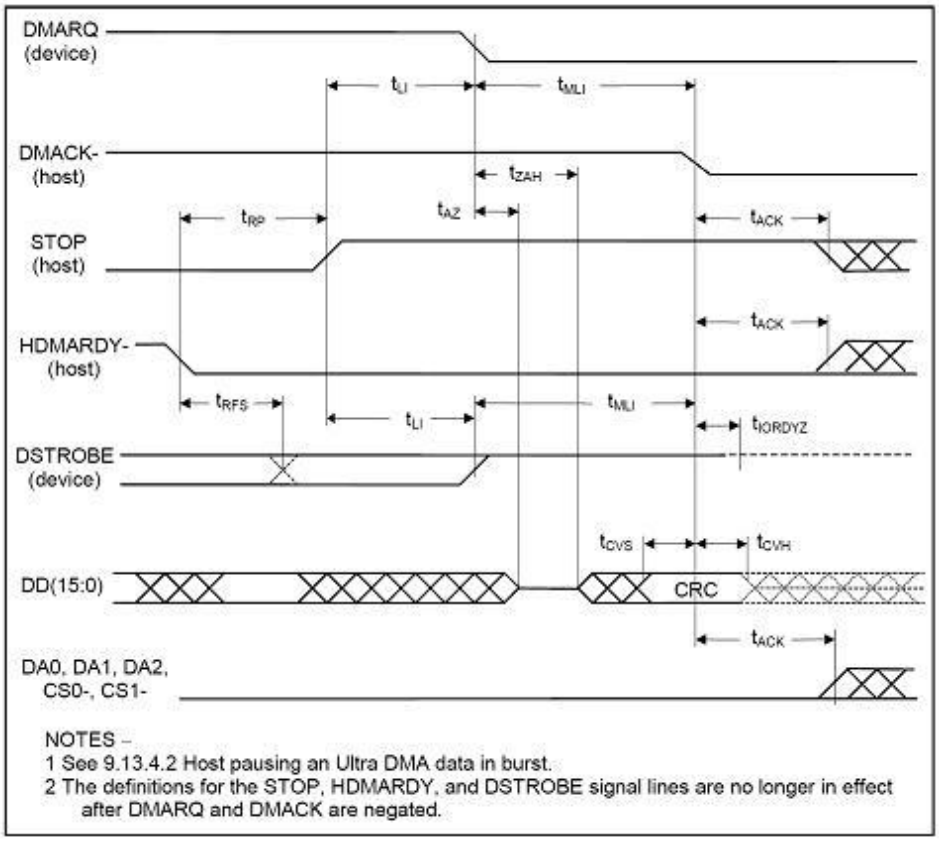
(Initialing an Ultra DMA data-in burst)



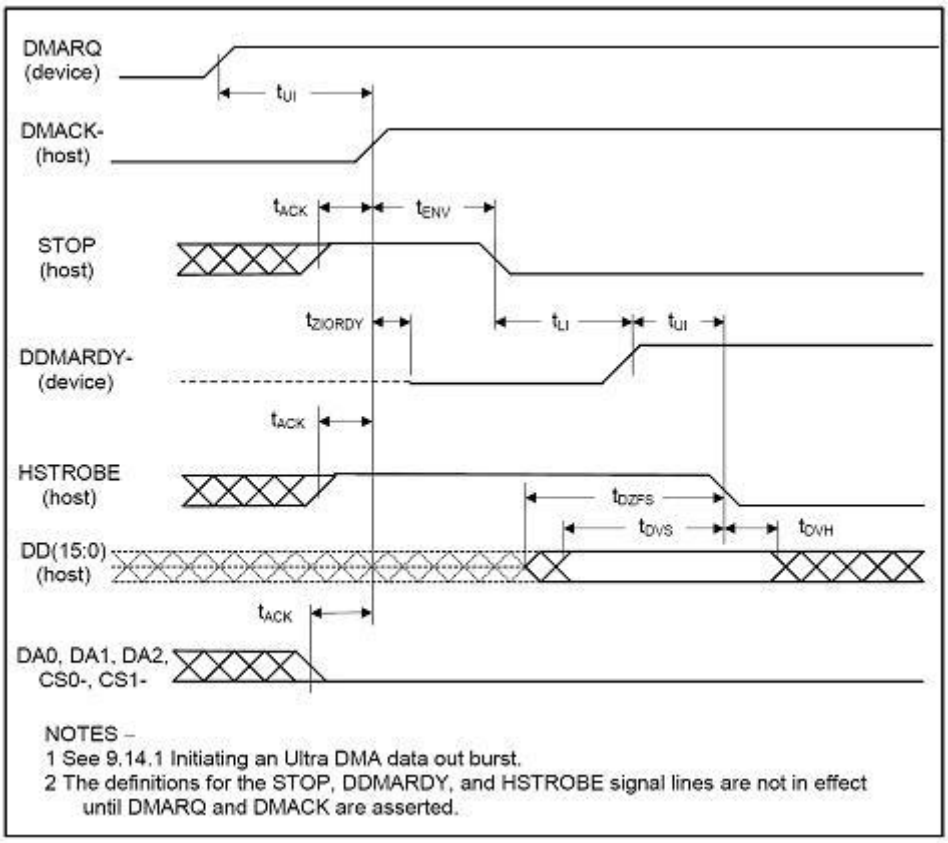
(Sustained Ultra DMA data-in burst)



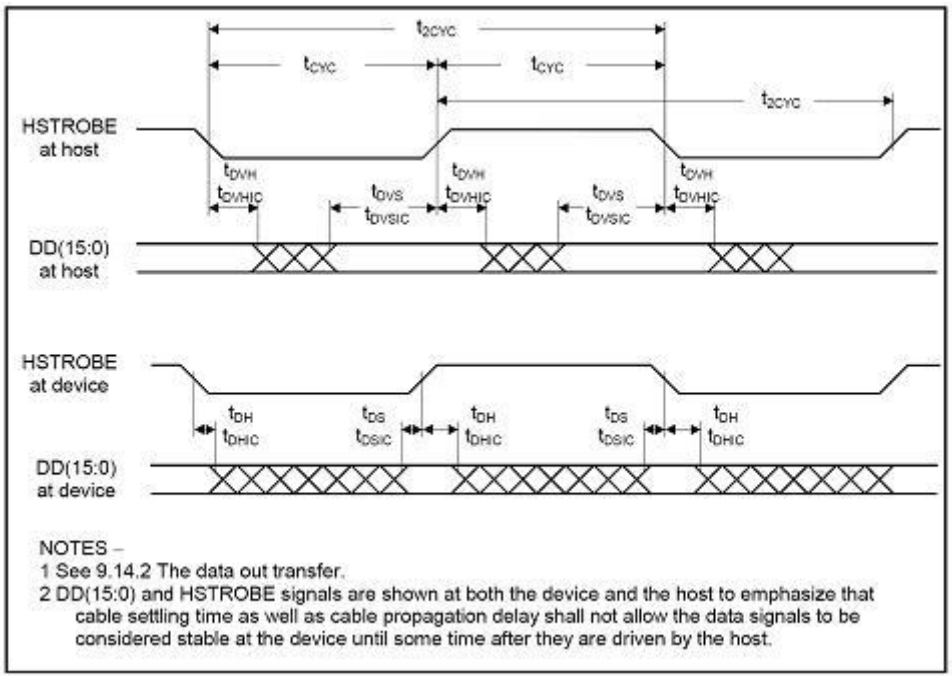
(Device terminating an Ultra DMA data-in burst)



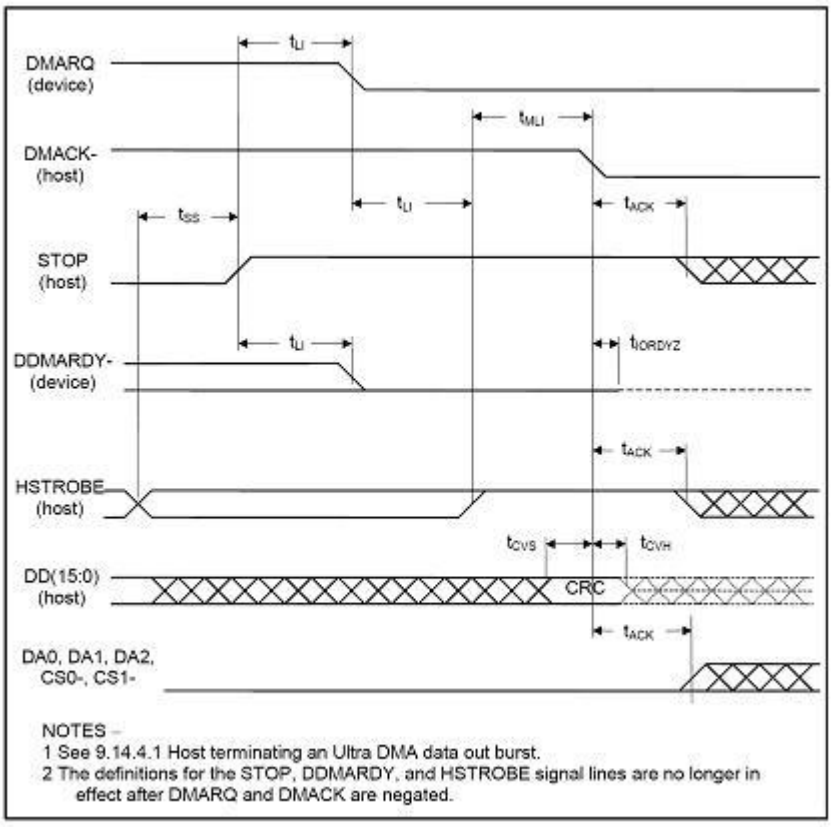
(Host terminating an Ultra DMA data-in burst)



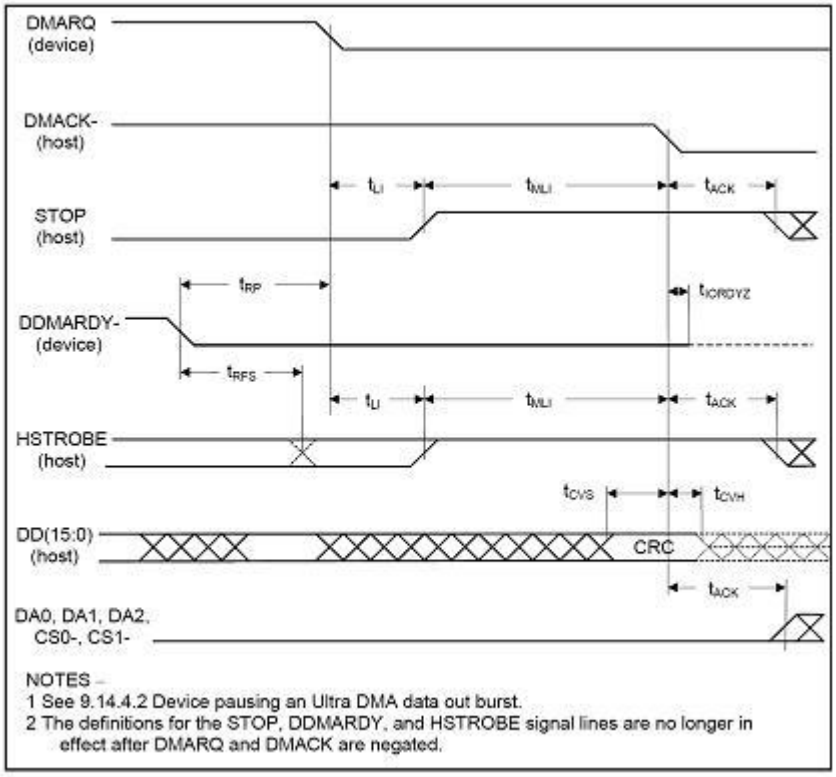
(Initialing an Ultra DMA data-out data burst)



(Sustained Ultra DMA data-out burst)



(Host terminating an Ultra DMA data-out burst)



(Device terminating an Ultra DMA data-out burst)

3.4 Power Management

System Power Consumption: **(Ta = 0 to 70^{0}C)**

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Iccr	Read current	5V	-	150	-	mA
Iccw	Write current	5V	-	130	-	mA
Ipd	Power down current	5V	-	12		mA
Iccr	Read current	3.3V	-	230	-	mA
Iccw	Write current	3.3V	-	200	-	mA
Ipd	Power down current	3.3V	-	18		mA

Note: Test Based on 8 pieces of TSOP flash.

4.0 Software Interface

4.1 ATA Task File Registers

The I/O decoding of each register is as follows

-CS1	-CS0	A2	A1	A0	-DIOR=0(-DIOW=1)	-DIOW=0(-DIOR=1)
1	0	0	0	0	Data(Read)	Data(Write)
1	0	0	0	1	Error	Feature
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector Number (LBA7-0)	Sector Number (LBA7-0)
1	0	1	0	0	Cylinder Low (LBA 15-8)	Cylinder Low (LBA 15-8)
1	0	1	0	1	Cylinder High (LBA 23-16)	Cylinder High(LBA 23-16)
1	0	1	1	0	Drive/Head (LBA 27-24)	Drive/Head (LBA 27-24)
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Drive Address	Reserved

4.2 Command Sets

Below table summarizes the PATA PCIe command set with the paragraphs that follow describing the individual commands and task file for each command.

No.	Command Set	Code	FR	SC	SN	CY	DR	HD	LBA
1	CFA Erase Sector(s)	C0h	--	Y	Y	Y	Y	Y	Y
2	CFA Request Extended Error Code	03h	--	--	--	--	Y	--	--
3	CFA Translate Sector	87h	--	Y	Y	Y	Y	Y	Y
4	CFA Write Multiple w/o Erase	CDh	--	Y	Y	Y	Y	Y	Y
5	CFA Write Sector w/o Erase	38h	--	Y	Y	Y	Y	Y	Y
6	Check Power Mode	E5h	--	--	--	--	Y	--	--
7	Execute Device Diagnostic	90h	--	--	--	--	Y	--	--
8	Identify Device	ECh	--	--	--	--	Y	--	--
9	Idle	E3h	--	Y	--	--	Y	--	--
10	Idle Immediate	E1h	--	--	--	--	Y	--	--
11	Initialize Device Parameters	91h	--	Y	--	--	Y	Y	--
12	NOP	00h	--	--	--	--	Y	--	--
13	Read Buffer	E4h	--	--	--	--	Y	--	--
14	Read DMA	C8h	--	Y	Y	Y	Y	Y	Y
15	Read Multiple	C4h	--	Y	Y	Y	Y	Y	Y
16	Read Sector(s)	20h	--	Y	Y	Y	Y	Y	Y
17	Read Verify Sector(s)	40h	--	Y	Y	Y	Y	Y	Y
18	Seek	70	--	--	Y	Y	Y	Y	Y
19	Set Features	EFh	Y	--	--	--	Y	--	--
20	Set Multiple Mode	C6h	--	Y	--	--	Y	--	--
21	Sleep	E6h	--	--	--	--	Y	--	--
22	Standby	E2h	--	--	--	--	Y	--	--
23	Standby Immediate	E0h	--	--	--	--	Y	--	--
24	Write Buffer	E8h	--	--	--	--	Y	--	--
25	Write DMA	CAh	--	Y	Y	Y	Y	Y	Y
26	Write Multiple	C5h	--	Y	Y	Y	Y	Y	Y
27	Write Sector(s)	30h	--	Y	Y	Y	Y	Y	Y

Note:

FR: Feature Register

SC: Sector Count Register

SN: Sector Number Register

HD: Head No. of Drive/Head Register

LBA: LBA mode supported

Y: Set up

CY: Cylinder Low/High Register --: Not set up

DR: Drive bit of Drive/Head register

4.3 Identify Drive Information

The Identity Drive Command enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero.

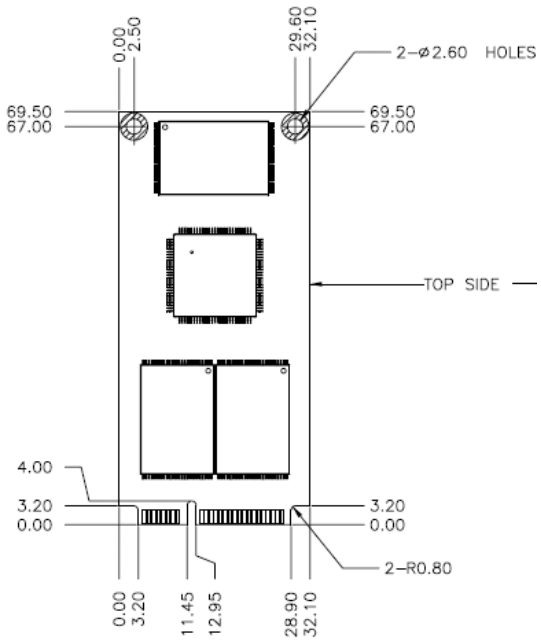
Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General configuration – bit significant for Non-removable device
1	xxxxh	2	Default number of cylinders
2	0000h	2	Reserved
3	xxxxh	2	Default number of heads
4	7E00h	2	Retired
5	0200h	2	Retired
6	xxxxh	2	Default number of sectors per track
7-8	xxxxh	4	Number of sectors per device
9	0000h	2	Retired
10-19	xxxxh	20	Serial Number in ASCII
20	0002h	2	Retired
21	0002h	2	Retired
22	0004h	2	Number of ECC Bytes passed on Read/Write Long Commands
23-26	Aaaah	8	Firmware revision in ASCII
27-46	xxxxh	40	Model number in ASCII
47	8001h	2	Maximum number of sector that shall be transferred on Read/Write Multiple commands
48	0000h	2	Reserved
49	2B00h	2	Capabilities-LBA/DMA Supported
50	4000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	Retired
53	0007h	2	Word 54-58, 64-70 and 88 are valid
54	xxxxh	2	Current numbers of cylinders
55	xxxxh	2	Current numbers of heads
56	xxxxh	2	Current sectors per track

Word Address	Default Value	Total Bytes	Data Field Type Information
57-58	Nnnnh	4	Current capacity in sectors (LBAs)(Word 57= LSW, Word 58= MSW)
59	0101h	2	Multiple sector setting is valid
60-61	Aaaah	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Retired
63	0n07h	2	Multiword DMA mode 2 and below are supported
64	0003h	2	Advance PIO transfer modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time 120nsec
66	0078h	2	Manufacturer's recommended Multiword DMA transfer cycle time 120nsec
67	0078h	2	Minimum PIO transfer cycle time without flow control 120nsec
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control 120nsec
69-81	0000h	26	Reserved
82	0002h	2	Supports Security Mode feature set
83-87	0000h	10	Reserved
88	0n7Fh	2	Ultra DMA mode 6 and below are supported
89-127	0000h	78	Reserved
128	0021h	2	Enhanced security erase supported
129-159	0000h	62	Reserved vendor unique bytes
160-255	0000h	192	Reserved

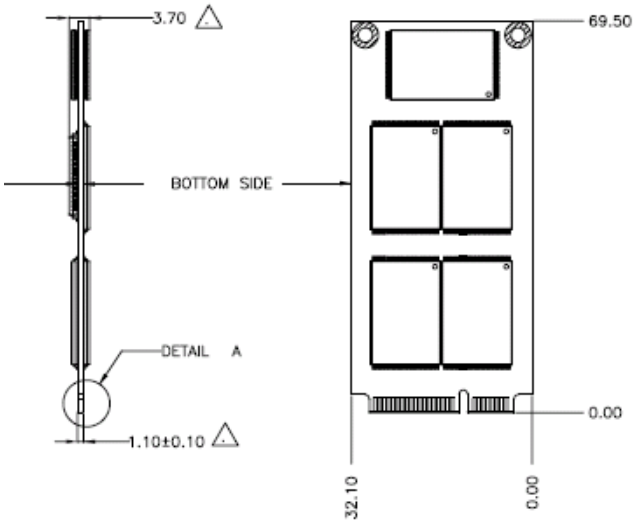
Note:

1. a = Vender Specific Configuration
2. n = Host Selectable Configuration

5.0 Physical Dimension



Top View



Side & Bottom View

Note: 1. Unit: mm

General Tolerance: ± 0.1

6.0 Weight

1) **8 TSOP Flash: 10.2g**
2) **4 TSOP Flash: 8.2g**
3) **2 TSOP Flash: 7.2g**
4) **1 TSOP Flash: 6.7g**